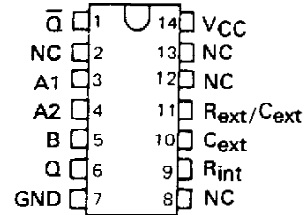
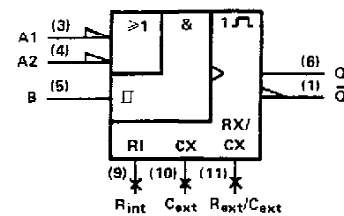


- Programmable Output Pulse Width  
With  $R_{int}$  . . . 35 ns Typ  
With  $R_{ext}/C_{ext}$  . . . 40 ns to 28 Seconds
- Internal Compensation for Virtual Temperature Independence
- Jitter-Free Operation up to 90% Duty Cycle
- Inhibit Capability

 SN54121 . . . J OR W PACKAGE  
 SN74121 . . . N PACKAGE  
 (TOP VIEW)


NC - No internal connection.

logic symbol<sup>‡</sup>
<sup>‡</sup>This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

INPUTS			OUTPUTS	
A1	A2	B	Q	$\bar{Q}$
L	X	H	L	H
X	L	H	L <sup>†</sup>	H <sup>†</sup>
X	X	L	L <sup>†</sup>	H <sup>†</sup>
H	H	X	L <sup>†</sup>	H <sup>†</sup>
H	L	H		
L	H	H		
L	L	H		
L	X	↑		
X	L	↑		

For explanation of function table symbols, see page

<sup>†</sup> These lines of the function table assume that the indicated steady-state conditions at the A and B inputs have been setup long enough to complete any pulse started before the setup.

## description

These multivibrators feature dual negative-transition-triggered inputs and a single positive-transition-triggered input which can be used as an inhibit input. Complementary output pulses are provided.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to  $V_{CC}$  noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 40 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e.,  $R_{int}$  connected to  $V_{CC}$ ,  $C_{ext}$  and  $R_{ext}/C_{ext}$  open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a d-c triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of  $V_{CC}$  and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and  $V_{CC}$  ranges for more than six decades of timing capacitance (10 pF to 10  $\mu$ F) and more than one decade of timing resistance (2 k $\Omega$  to 30 k $\Omega$  for the SN54121 and 2 k $\Omega$  to 40 k $\Omega$  for the SN74121). Throughout these ranges, pulse width is defined by the relationship  $t_{w(out)} = C_{ext}R_T \ln 2 \approx 0.7 C_{ext}R_T$ . In circuits where pulse cutoff is not critical, timing capacitance up to 1000  $\mu$ F and timing resistance as low as 1.4 k $\Omega$  may be used. Also, the range of jitter-free output pulse widths is extended if  $V_{CC}$  is held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended  $R_T$ . Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

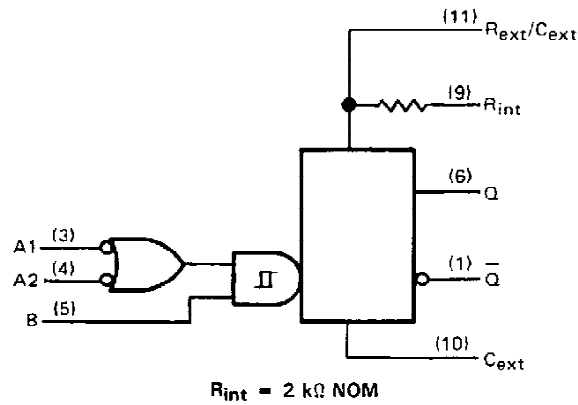
PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS  
INSTRUMENTS

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# SN54121, SN74121 MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

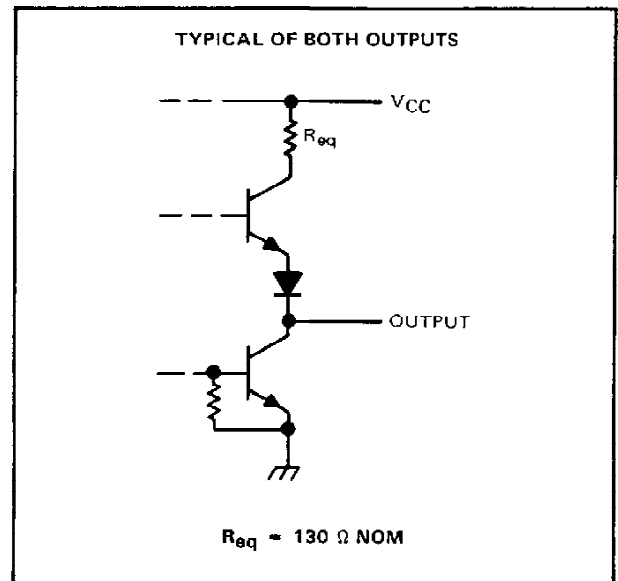
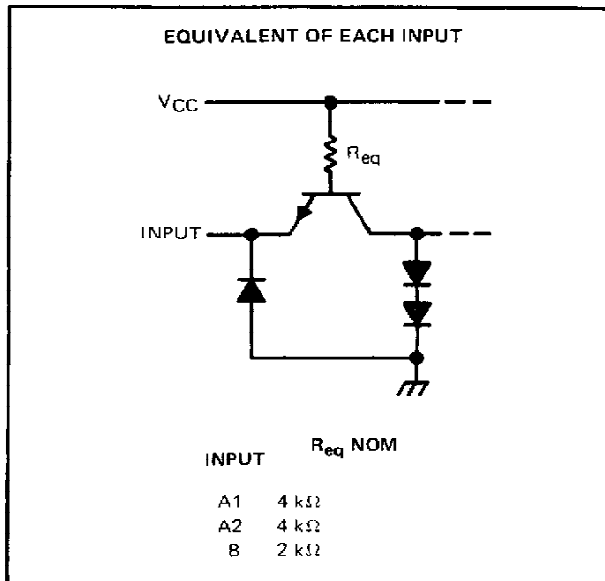
logic diagram (positive logic)



Pin numbers shown on logic notation are for J or N packages.

- NOTES: 1. An external capacitor may be connected between  $C_{ext}$  (positive) and  $R_{ext}/C_{ext}$ .  
2. To use the internal timing resistor, connect  $R_{int}$  to  $V_{CC}$ . For improved pulse width accuracy and repeatability, connect an external resistor between  $R_{ext}/C_{ext}$  and  $V_{CC}$  with  $R_{int}$  open-circuited.

## schematics of inputs and outputs



  
**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

# SN54121, SN74121 MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 3) .....	7 V
Input voltage .....	5.5 V
Operating free-air temperature range: SN54121 .....	-55 °C to 125 °C
SN74121 .....	0 °C to 70 °C
Storage temperature range .....	-65 °C to 150 °C

NOTE 3: Voltage values are with respect to network ground terminal.

**recommended operating conditions**

		MIN	NOM	MAX	UNIT	
$V_{CC}$	Supply voltage	54 Family	4.5	5	5.5	V
		74 Family	4.75	5	5.25	
$I_{OH}$	High-level output current			-0.4	mA	
$I_{OL}$	Low-level output current			16	mA	
dv/dt	Rate of rise or fall of input pulse	Schmitt input, B	1		V/s	
		Logic inputs, A1, A2	1		V/ $\mu$ s	
$t_{w(in)}$	Input pulse width		50		ns	
$R_{ext}$	External timing capacitance	54 Family	1.4	30	k $\Omega$	
		74 Family	1.4	40		
$C_{ext}$	External timing capacitance		0	1000	$\mu$ F	
	Duty cycle	$R_T = 2 \text{ k}\Omega$		67	%	
		$R_T = \text{MAX } R_{ext}$		90		
$T_A$	Operating free-air temperature	54 Family	-55	125	°C	
		74 Family	0	70		



# SN54121, SN74121 MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V <sub>IH</sub>	High-level input voltage at B input	V <sub>CC</sub> = MIN	2			V
V <sub>IL</sub>	Low-level input voltage at A input	V <sub>CC</sub> = MIN			0.8	V
V <sub>T+</sub>	Positive-going threshold voltage at B input	V <sub>CC</sub> = MIN		1.55	2	V
V <sub>T-</sub>	Negative-going threshold voltage at B input	V <sub>CC</sub> = MIN	0.8	1.35		V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA			-1.5	V
I <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX	2.4	3.4		V
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, I <sub>OL</sub> = MAX		0.2	0.4	V
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			1	mA
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V	A1 or A2		40	μA
			B		80	
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V	A1 or A2		-1.6	mA
			B		-3.2	
I <sub>OS</sub>	Short-circuit output current‡	V <sub>CC</sub> = MAX	54 Family	-20	-55	mA
			74 Family	-18	-55	
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = MAX	Quiescent	13	25	mA
			Triggered	23	40	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

†Not more than one output should be shorted at a time.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t <sub>PLH</sub>	Propagation delay time, low-to-high-level Q output from either A input	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 400 Ω, See Note 4	C <sub>ext</sub> = 80 pF, R <sub>int</sub> to V <sub>CC</sub>	45	70	ns	
t <sub>PLH</sub>	Propagation delay time, low-to-high-level Q output from B input			35	55	ns	
t <sub>PHL</sub>	Propagation delay time, high-to-low level Q̄ output from either A input			50	80	ns	
t <sub>PHL</sub>	Propagation delay time, high-to-low level Q̄ output from B input			40	65	ns	
t <sub>w(out)</sub>	Pulse width obtained using internal timing resistor		C <sub>ext</sub> = 80 pF, R <sub>int</sub> to V <sub>CC</sub>	70	110	150	ns
t <sub>w(out)</sub>	Pulse width obtained with zero timing capacitance		C <sub>ext</sub> = 0, R <sub>int</sub> to V <sub>CC</sub>	30	50	ns	
t <sub>w(out)</sub>	Pulse width obtained using external timing resistor		C <sub>ext</sub> = 100 pF, R <sub>T</sub> = 10 kΩ	600	700	800	ns
			C <sub>ext</sub> = 1 μF, R <sub>T</sub> = 10 kΩ	6	7	8	ms

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

TEXAS  
INSTRUMENTS

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# SN54121, SN74121 MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

## TYPICAL CHARACTERISTICS†

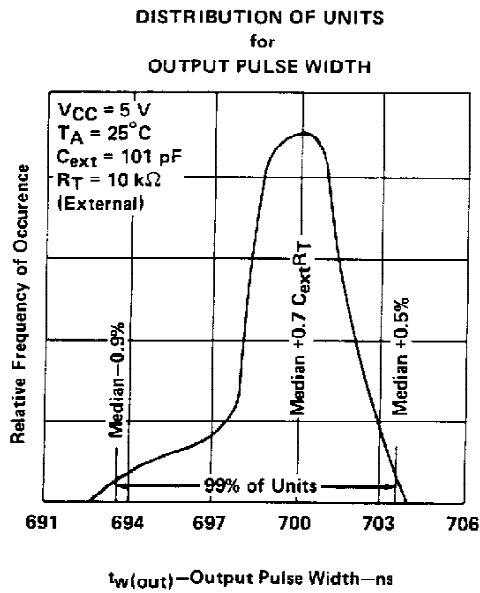


FIGURE 1

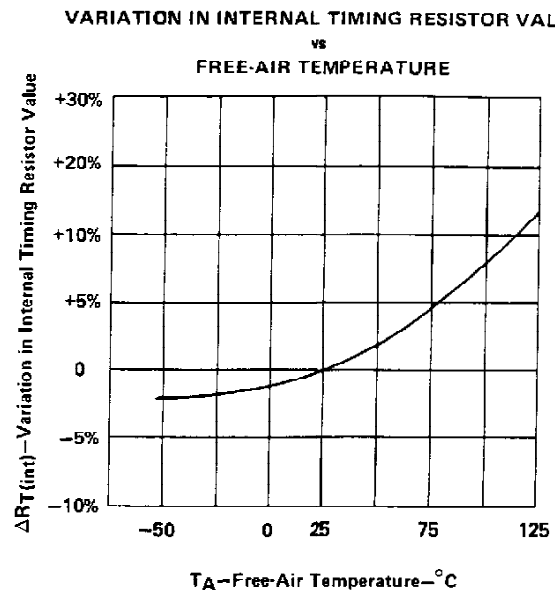


FIGURE 2

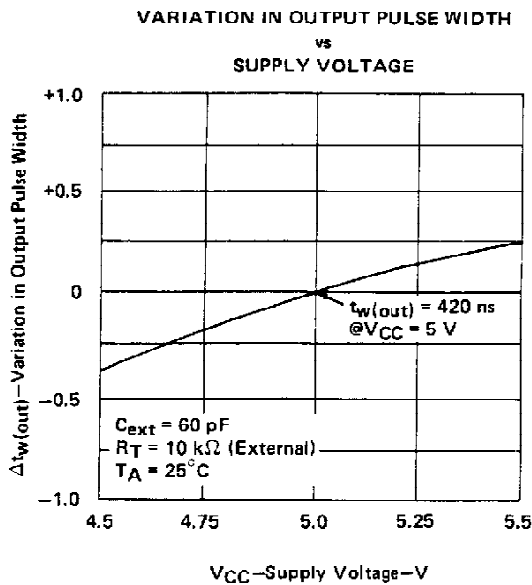


FIGURE 3

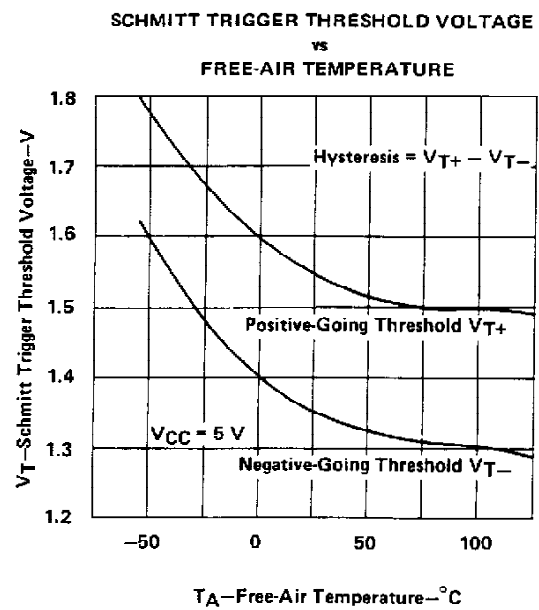


FIGURE 4

†Data for temperatures below 0°C and above 70°C are applicable for SN54121.

**SN54121, SN74121**  
**MONOSTABLE MULTIVIBRATORS**  
**WITH SCHMITT-TRIGGER INPUTS**

TYPICAL CHARACTERISTICS† (continued)

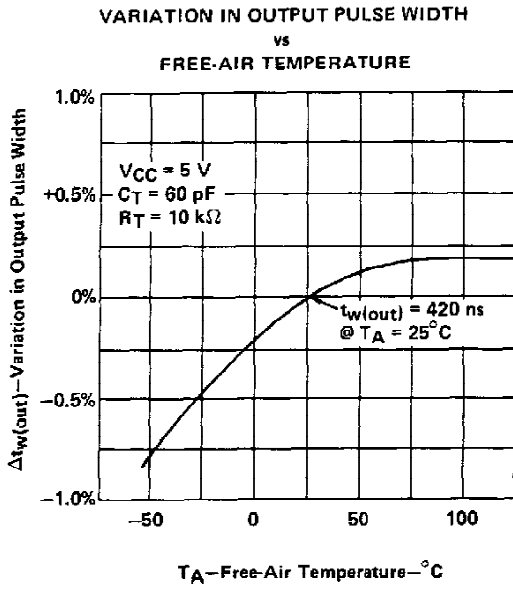


FIGURE 5

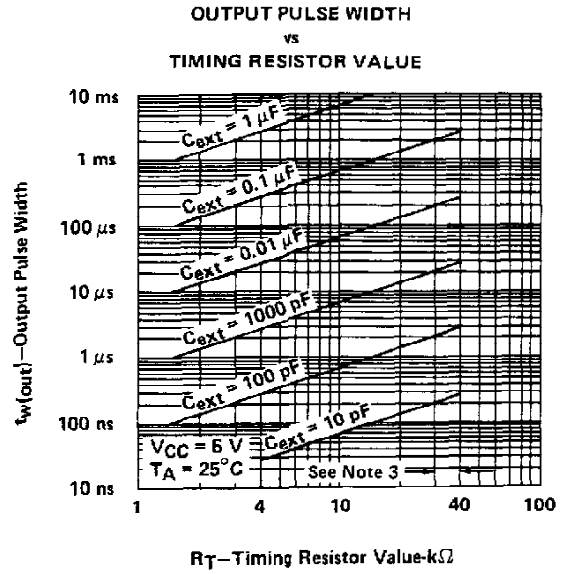


FIGURE 6

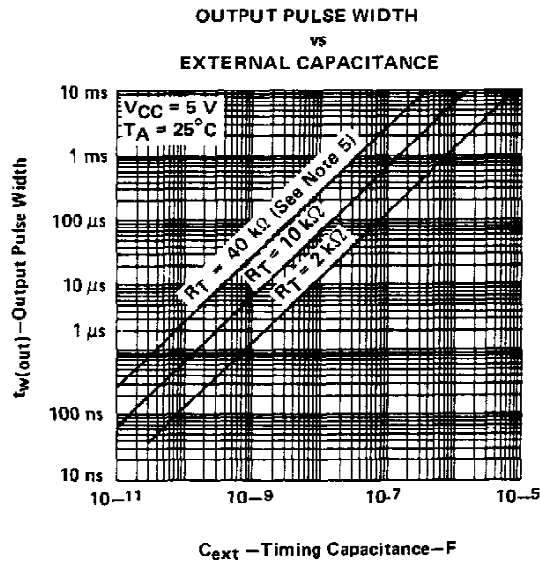


FIGURE 7

NOTE 5: These values of resistance exceed the maximum recommended use over the full temperature range of the SN54121.  
 †Data for temperatures below  $0^\circ\text{C}$  and above  $70^\circ\text{C}$  are applicable for SN54121.

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PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9755301QCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
5962-9755301QDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
5962-9755301QDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
SN54121J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SN54121J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SN74121D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74121D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74121DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74121DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74121N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74121N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74121N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74121N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74121NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74121NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SNJ54121J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54121J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54121W	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54121W	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54121WA	ACTIVE	CFP	WA	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54121WA	ACTIVE	CFP	WA	14	1	TBD	Call TI	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9755301QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9755301QC A SNJ54121J	<a href="#">Samples</a>
5962-9755301QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9755301QD A SNJ54121W	<a href="#">Samples</a>
SN54121J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54121J	<a href="#">Samples</a>
SN74121D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74121	<a href="#">Samples</a>
SN74121DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74121	<a href="#">Samples</a>
SN74121N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74121N	<a href="#">Samples</a>
SNJ54121J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9755301QC A SNJ54121J	<a href="#">Samples</a>
SNJ54121W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9755301QD A SNJ54121W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

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**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54121, SN74121 :**

- Catalog: [SN74121](#)
- Military: [SN54121](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

**NOTES:**

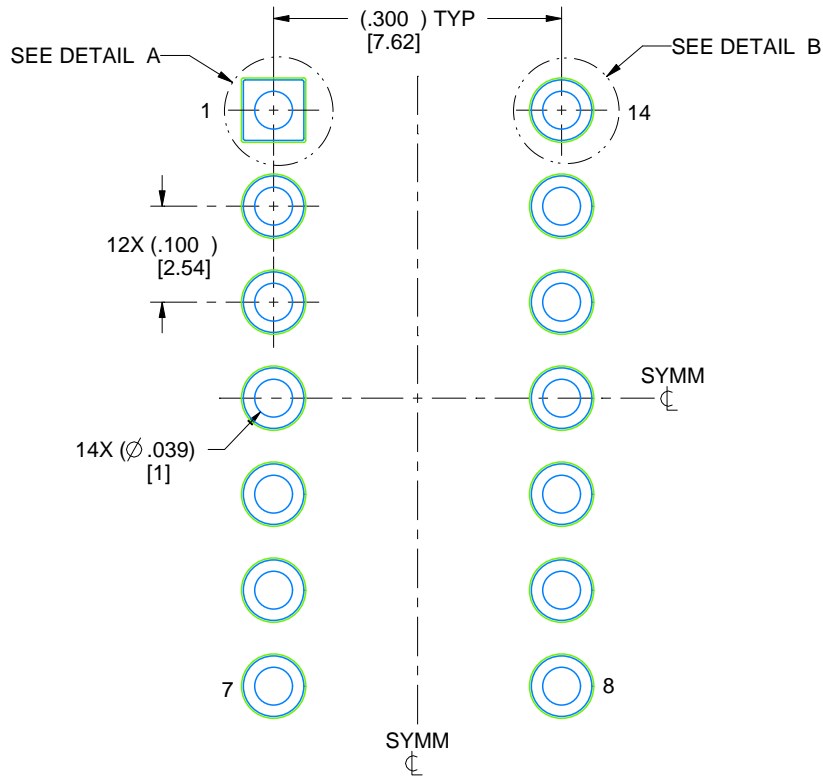
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



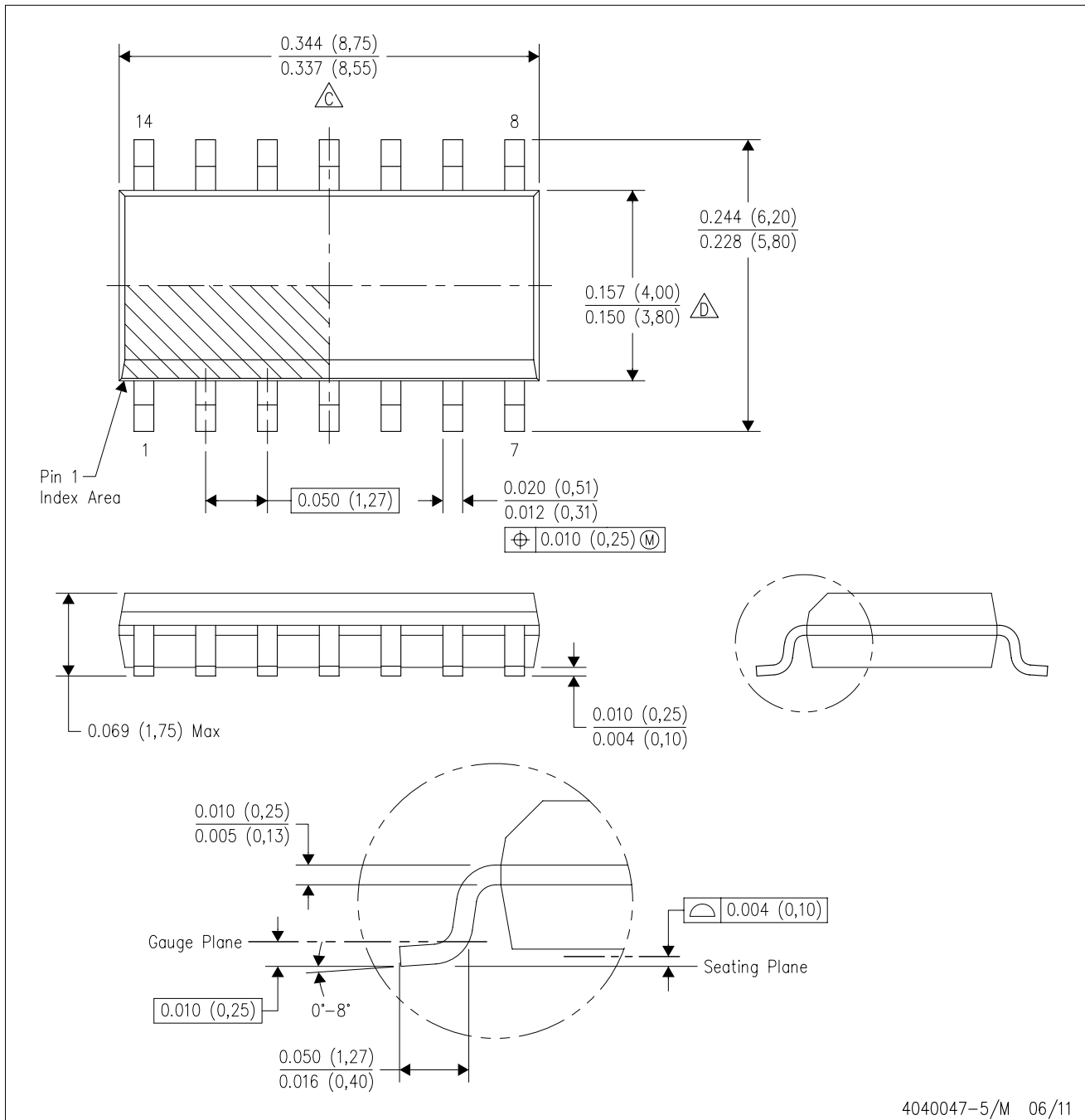
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X





4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

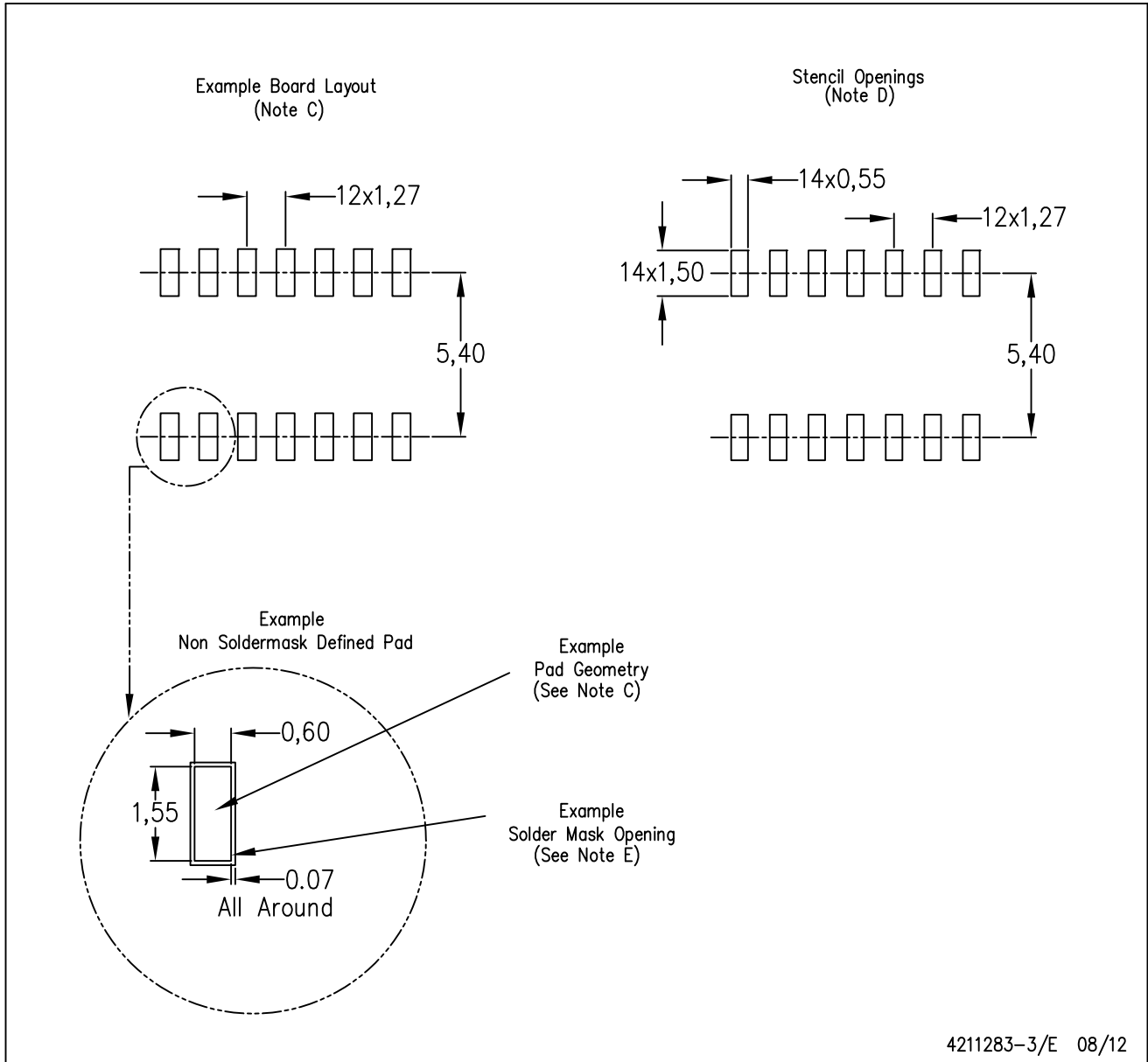


4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

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